Announcement of a contract for Senior Graduate or Engineer with Specialization in Analog Microelectronics.

The IFIC-Valencia and ETSE-University of Valencia announce the call for 1 contract with an extension of 2 years for a Senior Graduate or Engineer with Specialization in Analog Microelectronics. The contract is financed by the MCINN with European funds NextGenerationEU (PRTR-C17.I01) and by the Generalitat Valenciana in the Program of Complementary Plans for R+D+i in Astrophysics and High Energy Physics (ASFAE/2022/031).

The objective of the contract is to carry out R&D work on the design of a readout ASIC for the GRIT detector, in the context of the ASFAE/2022/031 project.

GRIT is a light charged particle detector with high granularity (high spatial resolution) with particle identification capability by the ΔE/E method and by pulse shape analysis (PSA). It will be used for studies of direct reactions in inverse kinematics with radioactive ion beams, provided by large European laboratories, and is designed to operate coupled to AGATA as well as other large Ge arrays. GRIT is designed and built by a collaboration between laboratories in Italy, France and Spain. GRIT has small dimensions, approximately 20 cm outer radius, but requires a high number of electronics channels (~8000), needed to encode the signals from the DSSD segmented detectors. The high number of channels, the small dimensions and the fact that it is compactly surrounded by other detectors, makes the design of the front-end electronics particularly challenging.

For the detector signals readout, one solution that has been evaluated is the use of analog memories in ASICs that can be installed in the vicinity of the detector. A first attempt to implement this idea was the prototype ASIC PLAS (PipeLined Asymmetric Switched Capacitor Array). The conceptual design of PLAS is published in **R. J. Aliaga, et al. Nucl. Instrum. Methods Phys. Res. A 800 (2015) 34.**

Presently, we have the second version of PLAS prototype, designed at IFIC and ETSE Valencia with 180 nm technology. The prototype ASIC was produced in the context of the international collaboration mentioned above, and in particular in close collaboration with the LPC laboratory in Caen, France, where the prototype has been characterized.

The prototype characterization has highlighted limitations and the design specifications for the readout ASIC, requested to be used in GRIT, have not been reached.

As mentioned above, the objective of this contract is the design of the GRIT readout ASIC and the tasks expected to be performed are:

- **Review of the current PLAS V2 design to assess whether the specifications in terms of ENOB (~11 bits) and analog sampling bandwidth (200 MHz) can be achieved improving the present design.**

- **Define the actions on the PLAS ASIC concept/implementation to achieve the required specifications for GRIT.**
- **Extension or modification of the PLAS V2 design to include a filter on the input signal or a method to use the ASIC pre-amplifier reset system to reduce baseline effects at high count rates.**
- **Definition and design of the ASIC test system and protocols.**

The work will be performed in an international collaborative environment, so stays at LPC Caen, France, INFN-Milano, Italy and other European laboratories are foreseen.

The initiative to undertake a PhD, with the new concepts that can be developed around the signal processing and the GRIT analog readout system will be highly appreciated.

Interested candidates can obtain more information about the different aspects of the project and of the contract by contacting:

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